IN THE CLAIMS:

1. (withdrawn) A method of forming a vertical transistor comprising the steps of:

providing a wafer having a layer of SiGe alloy above a bulk semiconductor substrate;

etching a trench through the layer of SiGe into the bulk substrate;

forming an isolating collar within the trench;

forming a lower contact for the vertical transistor above the isolating collar, the lower contact being in contact with a portion of the SiGe layer above the isolating collar;

forming an isolating layer within the trench overlapping vertically the lower contact;

forming a vertical body layer of silicon on an exposed vertical surface of the SiGe layer within the trench extending upward from the top surface of the isolating layer, whereby the layer of silicon is strained;

forming a gate dielectric on an exposed vertical surface of the silicon layer within the trench, thereby isolating the body layer from the trench interior;

forming a gate electrode within the trench separated from the body layer of silicon by the gate dielectric layer; and

forming an upper electrode of the transistor in contact with the body layer of silicon, thereby establishing a path for conducting carriers from said lower contact to said upper contact through said vertical body layer.

2. (withdrawn) A method according to claim 1, in which said SiGe layer is separated from said bulk substrate by a buffer layer of SiGe.

3. (withdrawn) A method according to claim 1, in which said body layer of silicon is formed under an overhang of a pad dielectric and extending out into said trench to said original trench width;
further comprising a step of etching a portion of said gate electrode extending up to a wafer surface to leave a central gate electrode of width less than said original trench width, said central gate electrode having at least one aperture adjacent thereto that extends outward to said original trench width and down to make contact with said upper electrode; and
filling said aperture with dielectric to isolate said central gate electrode.

4. (withdrawn) A method according to claim 3, further comprising a step of forming a gate contact on said central gate electrode, capped by a gate contact cap and bracketed by gate contact sidewalls; and
forming an aperture for a drain contact adjacent to one of said gate contact sidewalls, said aperture being located transversely with respect to said central

gate electrode to make contact with said vertical body layer and with said drain.

5. (withdrawn) A method according to claim 2, in which said body layer of silicon is formed under an overhang of a pad dielectric and extending out into said trench to said original trench width;
further comprising a step of etching a portion of said gate electrode extending up to a wafer surface to leave a central gate electrode of width less than said original trench width, said central gate electrode having at least one aperture adjacent thereto that extends outward to said original trench width and down to make contact with said upper electrode; and
filling said aperture with dielectric to isolate said central gate electrode.

6. (withdrawn) A method according to claim 5, further comprising a step of forming a gate contact on said central gate electrode, capped by a gate contact cap and bracketed by gate contact sidewalls; and
forming an aperture for a drain contact adjacent to one of said gate contact sidewalls, said aperture being located transversely with respect to said central gate electrode to make contact with said vertical body layer and with said drain.

7. (withdrawn) A method of forming a DRAM cell having a vertical transistor comprising the steps of:

providing a wafer having a layer of SiGe alloy above a bulk semiconductor substrate;

etching a trench having an original trench width through the layer of SiGe into the bulk substrate;

forming a capacitor within a lower portion of said trench;

forming an isolating collar within said trench above said capacitor;

forming a lower contact for the vertical transistor above said isolating collar, said lower contact being in contact with a portion of the SiGe layer above the isolating collar;

forming an isolating layer within the trench overlapping vertically the lower contact, thereby separating said capacitor from an upper portion of said trench;

depositing epitaxially a vertical body layer of silicon on an exposed vertical surface of said SiGe layer within the trench extending upward from the top surface of the isolating layer, whereby said body layer of silicon is strained;

forming a gate dielectric on an exposed vertical surface of said silicon body layer within the trench, thereby isolating said silicon body layer from the trench interior;

forming a gate electrode within the trench and separated from said body layer of silicon by said gate dielectric layer; and

forming an upper electrode of a FET transistor in contact with said body layer of silicon, thereby establishing a path for electrons from said lower contact to said upper contact through said vertical body layer.

8. (withdrawn) A method according to claim 7, in which said SiGe layer is separated from said bulk substrate by a buffer layer of SiGe.

9. (withdrawn) A method according to claim 7, in which said body layer of silicon is formed under an overhang of a pad dielectric and extending out into said trench to said original trench width;

further comprising a step of etching a portion of said gate electrode extending up to a wafer surface to leave a central gate electrode of width less than said original trench width, said central gate electrode having at least one aperture adjacent thereto that extends outward to said original trench width and down to make contact with said upper electrode.

10. (withdrawn) A method according to claim 9, in which said at least one aperture has a width extending outward from said central gate electrode

to said body layer, thereby defining a boundary of a bitline contact extending outwardly from said aperture;

said at least one aperture is filled with a layer of array top dielectric extending up to a top surface of said central gate electrode;

said top surface of said central gate electrode is extended above said top surface in a gate contact;

sidewall spacers are formed on said gate contact;

a bitline contact aperture is etched extending outward from said sidewall spacers on said gate contact.

11. (withdrawn) A method according to claim 8, in which said body layer of silicon is formed under an overhang of a pad dielectric and extending out into said trench to said original trench width;

further comprising a step of etching a portion of said gate electrode extending up to a wafer surface to leave a central gate electrode of width less than said original trench width, said central gate electrode having at least one aperture adjacent thereto that extends outward to said original trench width and down to make contact with said upper electrode.

12. (withdrawn) A method according to claim 11, in which said at least one aperture has a width extending outward from said central gate electrode

to said body layer, thereby defining a boundary of a bitline contact extending outwardly from said aperture;

said at least one aperture is filled with a layer of array top dielectric extending up to a top surface of said central gate electrode;

said top surface of said central gate electrode is extended above said top surface in a gate contact;

sidewall spacers are formed on said gate contact;

a bitline contact aperture is etched extending outward from said sidewall spacers on said gate contact.

13. (currently amended) An integrated circuit structure comprising a vertical transistor comprising:

a semiconductor wafer having a layer of SiGe alloy above and substantially parallel to a bulk semiconductor substrate;

said wafer having a trench etched through the layer of SiGe into the bulk substrate;

an isolating collar formed within the trench;

a lower contact for the vertical transistor formed above the isolating collar, the lower contact being in contact with a portion of the SiGe layer above the isolating collar;

a vertical body layer of strained silicon formed on an exposed vertical surface of the SiGe layer within the trench, said exposed vertical surface being recessed transversely from an original trench width, and said body layer extending upward substantially at said original trench width from the top surface of the lower contact, whereby the body layer of silicon is strained;

a gate dielectric layer formed on an exposed vertical surface of the silicon body layer within the trench, thereby isolating the body layer from the trench interior;

a gate electrode formed within the trench and separated from the body layer of silicon by the gate dielectric layer; and

an upper electrode of the transistor formed in contact with the body layer of silicon, thereby establishing a path for conducting carriers from said lower contact to said upper contact through said vertical body layer.

14. (original) A structure according to claim 13, in which said SiGe layer is a fully relaxed layer separated from a silicon bulk substrate by a buffer layer of SiGe.

15. (original) A structure according to claim 13, in which said body layer of silicon is formed under an overhang of a pad dielectric and extending out into said trench to said original trench width;

further comprising a portion of said gate electrode extending up to a wafer surface thereby leaving a central gate electrode of width less than said original trench width, said central gate electrode having at least one aperture adjacent thereto that extends outward to said original trench width and down to make contact with said upper electrode; and

dielectric filling said aperture adjacent to said central gate electrode to isolate said central gate electrode.

16. (original) A structure according to claim 15, further comprising a gate contact formed on said central gate electrode, capped by a gate contact cap and bracketed by gate contact sidewalls; and

an aperture for a drain contact formed adjacent to one of said gate contact sidewalls, said aperture being located transversely with respect to said central gate electrode to make contact with said vertical body layer and with said drain.

17. (original) A structure according to claim 14, in which said body layer of silicon is formed under an overhang of a pad dielectric and extending out into said trench to said original trench width;

further comprising a portion of said gate electrode extending up to a wafer surface thereby leaving a central gate electrode of width less than said

original trench width, said central gate electrode having at least one aperture adjacent thereto that extends outward to said original trench width and down to make contact with said upper electrode; and

dielectric filling said aperture adjacent to said central gate electrode to isolate said central gate electrode.

18. (original) A structure according to claim 17, further comprising a gate contact formed on said central gate electrode, capped by a gate contact cap and bracketed by gate contact sidewalls; and

an aperture for a drain contact formed adjacent to one of said gate contact sidewalls, said aperture being located transversely with respect to said central gate electrode to make contact with said vertical body layer and with said drain.

19. (Previously presented) An integrated circuit containing at least one DRAM cell having a vertical transistor comprising:

a wafer having a layer of SiGe alloy above a bulk semiconductor substrate;

a trench having an original trench width extending down through the layer of SiGe into the bulk substrate;

a capacitor formed within a lower portion of said trench;

an isolating collar formed within said trench above said capacitor;

a lower contact for the vertical transistor formed above said isolating collar, said lower contact being in contact with a portion of the SiGe layer above the isolating collar;

an isolating layer formed within the trench overlapping vertically the lower contact, thereby separating said capacitor from an upper portion of said trench;

a vertical body layer of strained silicon disposed on an exposed vertical surface of said SiGe layer within the trench, said exposed vertical surface being recessed transversely from an original trench width, and extending upward substantially at said original trench width from the top surface of the isolating layer, whereby said body layer of silicon is strained;

a gate dielectric formed on an exposed vertical surface of said silicon body layer within the trench, thereby isolating said silicon body layer from the trench interior;

a gate electrode formed within the trench and separated from said body layer of silicon by said gate dielectric layer; and

an upper electrode of a FET transistor in contact with said body layer of silicon, thereby establishing a path for electrons from said lower contact to said upper contact through said vertical body layer.

20. (previously presented) A circuit according to claim 19, in which said SiGe layer is a fully relaxed layer separated from a silicon bulk substrate by a buffer layer of SiGe.

21. (previously presented) A circuit according to claim 19, in which said body layer of silicon is formed under an overhang of a pad dielectric and extending out into said trench to said original trench width;
further comprising a portion of said gate electrode extending up to a wafer surface thereby leaving a central gate electrode of width less than said original trench width, said central gate electrode having at least one aperture adjacent thereto that extends outward to said original trench width and down to make contact with said upper electrode; and
dielectric filling said aperture adjacent to said central gate electrode to isolate said central gate electrode.

22. (previously presented) A circuit according to claim 21, further comprising a gate contact formed on said central gate electrode, capped by a gate contact cap and bracketed by gate contact sidewalls; and
an aperture for a drain contact formed adjacent to one of said gate contact sidewalls, said aperture being located transversely with respect to said central

gate electrode to make contact with said vertical body layer and with said drain.

23. (previously presented) A circuit according to claim 20, in which said body layer of silicon is formed under an overhang of a pad dielectric and extending out into said trench to said original trench width;

further comprising a portion of said gate electrode extending up to a wafer surface thereby leaving a central gate electrode of width less than said original trench width, said central gate electrode having at least one aperture adjacent thereto that extends outward to said original trench width and down to make contact with said upper electrode; and

dielectric filling said aperture adjacent to said central gate electrode to isolate said central gate electrode.

24. (previously presented) A circuit according to claim 23, further comprising a gate contact formed on said central gate electrode, capped by a gate contact cap and bracketed by gate contact sidewalls; and

an aperture for a drain contact formed adjacent to one of said gate contact sidewalls, said aperture being located transversely with respect to said central gate electrode to make contact with said vertical body layer and with said drain.

25. (previously presented) A circuit according to claim 19, in which said at least one DRAM cell comprises an array of DRAM cells.

26. (previously presented) A circuit according to claim 25, in which said circuit comprises a dynamic random access memory having an array of DRAM cells.